Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("—"), as is applicable:

1. (Previously presented) A method for evaluating a processor design, the method comprising:

testing a lot of wafers at two or more voltage levels;

collecting test results from the testing of the lot of wafers in a test results file;

searching the test results file that contains the test results for the lot of wafers at the two or more voltage levels; and

determining an optimal operational voltage based on test failures indicated in the test results.

2. (Previously presented) The method of claim 1, wherein the searching the test results file comprises parsing the file.

3. (Previously presented) The method of claim 1, wherein the searching the test results file comprises opening the file and parsing the file.

4. (Original) The method of claim 1, wherein the determining an optimal operational voltage comprises:

determining the number of test failures at a first voltage level;

determining the number of test failures at a second voltage level; and

determining which of the first voltage level and the second voltage level had the least test failures.

5. (Previously presented) The method of claim 1, wherein the searching the test results file comprises decompressing the file.

6. (Previously presented) A system for evaluating a processor design, the system comprising:

a component configured to test a lot of wafers at two or more voltage levels and collect test results from the testing of the lot of wafers in a test results file;

a parser module configured to search the test results file that contains the test results for the lot of wafers at the two or more voltage levels;

a test failure calculation module configured to determine test failures that occurred at the two or more voltage levels; and

an optimal operational voltage module configured to determine which of the two or more voltage levels is optimal.

7. (Previously presented) The system of claim 6, wherein the parser module is configured to open the test results file.

8. (Original) The system of claim 6, wherein the parser module, the test failure calculation module, and the optimal operational voltage module comprise software that is executed by a processor.

9. (Previously presented) The system of claim 6, wherein the parser module is configured to decompress the test results file.

10. (Original) The system of claim 6, wherein the parser module, the test failure calculation module, and the optimal operational voltage module comprise a PERL script.

11. (Previously presented) A computer program embodied in a computer-readable medium for evaluating a processor design, the program comprising:

logic configured to test a lot of wafers at two or more voltage levels and collect test results from the testing of the lot of wafers in a test results file;

logic configured to search the test results file that contains the test results for the lot of wafers at the two or more voltage levels; and

logic configured to determine an optimal operational voltage based on test failures indicated in the test results.

12. (Previously presented) The program of claim 11, wherein the logic configured to search is further configured to decompress the test results file.

13. (Previously presented) The program of claim 12, wherein the logic configured to search is further configured to parse the test results file.

14. (Original) The program of claim 11, wherein the logic configured to determine an optimal operational voltage comprises logic configured to:

determine the number of test failures at a first voltage level;

determine the number of test failures at a second voltage level; and

determine which of the first voltage level and the second voltage level had the least test failures.

15. (Previously presented) A system for evaluating a processor design, the system comprising:

means for testing a lot of wafers at two or more voltage levels;

means for collecting test results from the testing of the lot of wafers in a test results file;

means for searching the test results file that contains the test results for the lot of wafers at the two or more voltage levels; and

means for determining an optimal operational voltage based on test failures indicated in the test results.

16. (Previously presented) The method of claim 1, wherein determining an optimal operational voltage comprises determining the relative significance of the test failures and determining the optimal operational voltage based upon the relative significance.

17. (Previously presented) The system of claim 6, wherein the optimal operation voltage module is configured to determine the number of test failures at a first voltage level, determine the number of test failures at a second voltage level, and determine which of the first voltage level and the second voltage level had the least test failures.

18. (Previously presented) The system of claim 6, wherein the optimal operation voltage module is configured to determine the relative significance of the test failures and determine the optimal operational voltage based upon the relative significance.

19. (Canceled)

20. (Previously presented) The system of claim 15, wherein the means for determining an optimal operational voltage comprise means for determining the number of test failures at a first voltage level, determining the number of test failures at a second voltage level, and determining which of the first voltage level and the second voltage level had the least test failures.

21. (Previously presented) The system of claim 15, wherein the means for determining an optimal operational voltage comprise means for determining the relative significance of the test failures and determining the optimal operational voltage based upon the relative significance.